Gold Wire bonding

Introduction

Wire bonding is the main method for contacting of integrated circuits (IC), LED, sensors or mircro- electro-mechanical-systems (MEMS) to a substrate or to other dice. Among the many chip assembling technologies, wire bonding is undquestionably the most fascinating but also the most challenging one.

BALL-WEDGE Wire Bonding is the most common wire bond method due to its highly flexible process. One of the key advantages of ball-wedge bonding is the ability to quickly produce test samples for evaluations purpose using standardised IC substrates. Wire bonding is, therefore, suited for both, prototyping as well as for fully automated mass production.

Wire bonding is only one of the different processes within a long IC assembly chain. It starts with an appropriate substrate design, a ball bond and wire specific coating and ends with functional testing of the assembled devices.

Our service includes all processes, from substrate layouting, Die- and wire bonding, plasma cleaning, encapsulation to final testing.

Different types of automated wire bonders equipped with different options allow us to satisfy all customer needs. We can assemble all common substrates, from very thin flex pcb to very thick metalcore PCB, Ceramic, Saphire, Rigid Flex and so on.

Thanks to our close relationship and collaboration with PCB suppliers, coating services and Universtities, we also develop new wire bonding processes for any kind of special applications.

In the following we report on some selected wire bonding applications that go over a simple ball wedge bond connection.

Fine Pitch

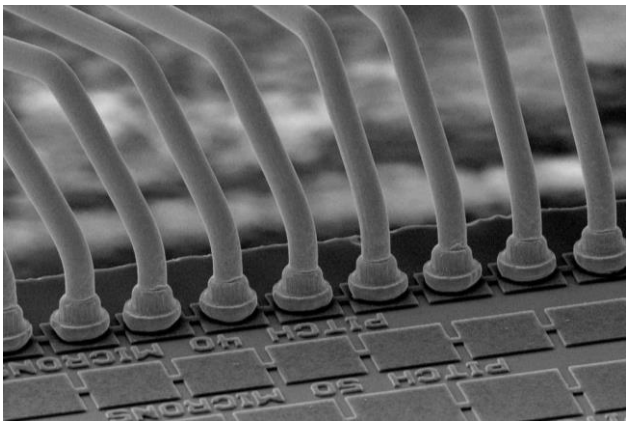

Figure 1: Ultra Fine Pitch (40um) wire bonding

When many wires must be bonded or space for connections is limited for any reason, fine pitch wire bonding is required. Fine pitch and ultra fine pitch are denoted for pitches smaller than 80um and 50um, respectively.

The main challenges are the evaluation of a suitable capillary and wire type. In addition, also substrate layout and coating must match the requirements for a fine pitch process, in order to achieve a reliable wire bonding.

A systematical DOE, modern wire bonders, quality control - and plasma cleaning equipments along with an extensive experience in optimizing a wire bonding process are further, crucial elements necessary for a complete service.

Staggered Wires

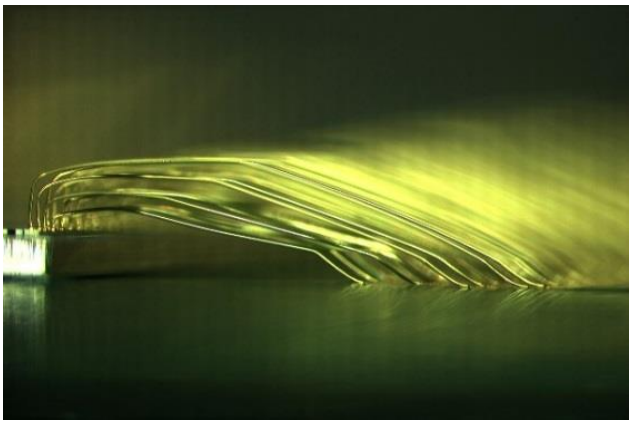

Figure 2: Four level stggered loop wire bonding of a line camera sensor

Especially when the I/O number is very large, wires a so-called staggered wire bonding process is needed. Wires are then distributed over two or more levels. In order to achieve the required mechanical stability, low loop height variation and low wires sway, wires types with dedicated mechanical characteristics must be evaluated.

Loop setup turns out to be the very challenge, especially when bonding is done on Ball Grid Array (BGA) substrates with very long wires.

On our machines, devices with up to 1000 wires can automaticalle be processed at a very high speed.

Chip scale Wire bonding

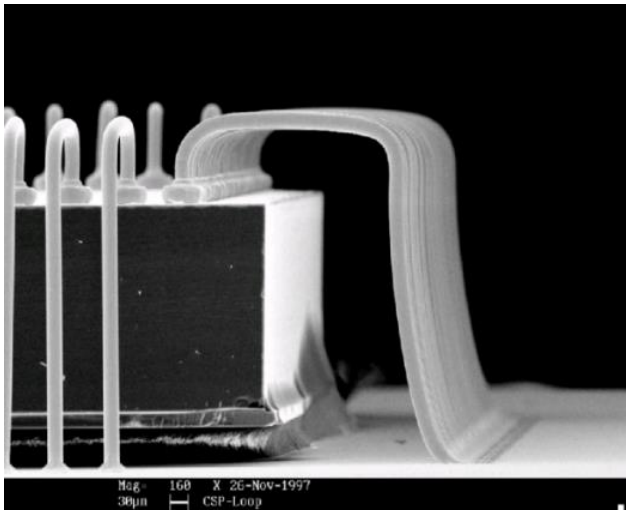

Figure 3: Chip scale packaging wire loop shape

A so-called Chip Scale Package (CSP) is a type of IC package, where its area is not larger than 20% of the die size. CSP assembly starts with an adequate die bonding process. Apart from precise positioning of the die, the charactersitic of the die bonding glue is essential. If bleed out is to strong, wire bonding is not reliable.

Evaluation of the wire – and capillary type are additional challenges, that must be solved by the process engineer.

Even more difficulties may arise when the die is bonded into a cavity. The required space for loop shape formation is then further limited by the cavity walls,

J-Loop wire bonding

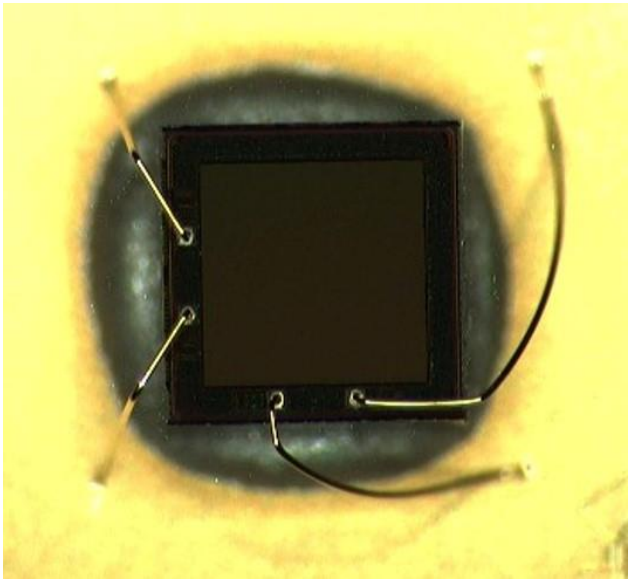

Figure 4: J-Loop wire bonding of a micro camera sensor

J-Loops or also called „smart Loops“ are typically used in smart card applications with low loop heights. However, the may also be needed, for test sample production, where the substrate layout does not suit the pad layout of the die, as shown for example in Fig.4 for a micro camera application. For technical reasons, wires can not be bonded over the sensor area and must therefore be fed around the corner, resulting in a J shape of the bonded wires.

J-Loops are also used, when LED packages with many different LED dice. In order to minimize shadowing, wires are bonded such, to not Ball.

Ultra low loop:

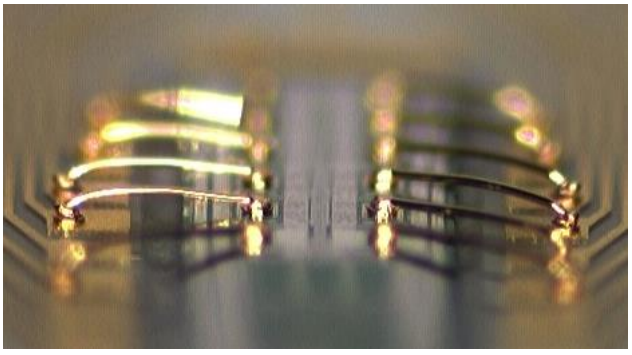

Figure 5: Ultra flat loop wire bonding with a loop heigt of 150um

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Ultra low loop wire bonding is another feature offered by our wire bonding service. This technology allows to further reduce packaging size, similar CSP Bonding, but in z-direction.

Mobile phone industry is probably the main driver for this low loop technology. Unlra flat loops are e.g. required for stacked dice packages.

Ultra low loops may, however, also be of interst for sensor application, where package height must be kept as small as possible, in order to increase its sensitivity.

Depending on the wire lenght, height of ultra flat loops can be sized dowh to 150um as shown in Fig. 5.

Ball Bumping

Figure 7: Ball bumps wire bonded on a silicon die

In the ball- or stud bumping process, instead of unthreading the wire to form a loop, the second connection is placed directly to the ball.

Ball bumps are typically used for flip chip applications, as security bond for wedge bonds, or as coating on die pads for chip to chip bonding. However, in micro system technology ball bumps may be used for a variaty of special applications, like e.g. as precise spacer for any assembly processes.

In combination with a shear tester, the height of as-produced ball bumps can even be adjusted even at the micrometer level.

Die-to-Die wire bonding

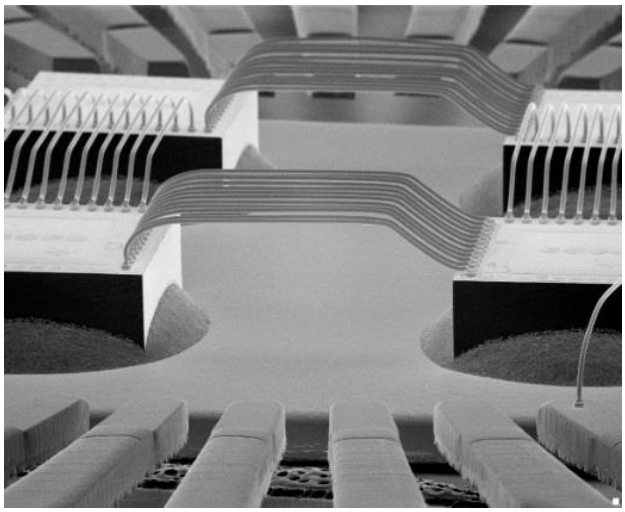

Figure 8: Die-to-Die wire bonding of dummy chips

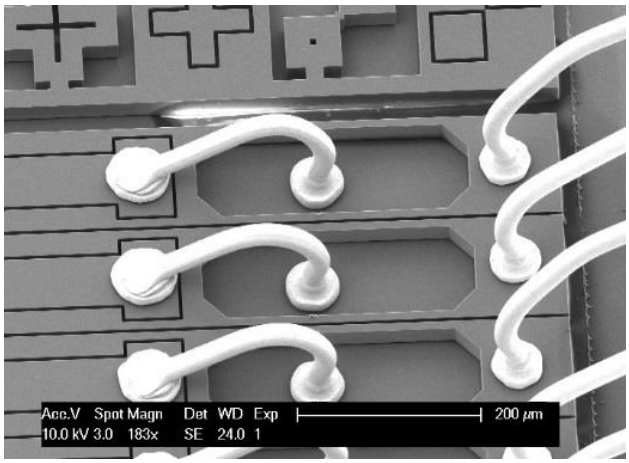

Figure 6: Die-to-Die wire bonding of a MEMS device

Die to Die wire bonding is a very useful techniques to flexibly connect dice with each other without the use of a substrate as interface layer. Due to the direct contact, die can be placed very close increasing the integration density and saving substrate space.

Die to Die wire bonding may also be used for high frequency applications, where interconnection length must be kept as short as possible.

A special example of die-to-die wire bonding is shown in Fig. 7. In this application, wires do not connect different devices, but different layers of the same MEMS device.

Substrate

Each type of appliction needs the right substrate. We process all common substrates, such as FR4, FR5, Rigid-Flex, Flex, IMS, Rogers, Saphire as well as thin-film, thick-film and DCB ceramics.

The wirebonding areas is 2x2 inch. Substrate can be Strips or Single packages, that are transported using boat carrier.
In case of very sophisticated packages, which can not be handeld by an indexeer, our machines can be run in a half automatic mode.
This way also non-standard devices can be wire bonded using all the options offerd by a high technology wire bonder.

Plasma cleaning:

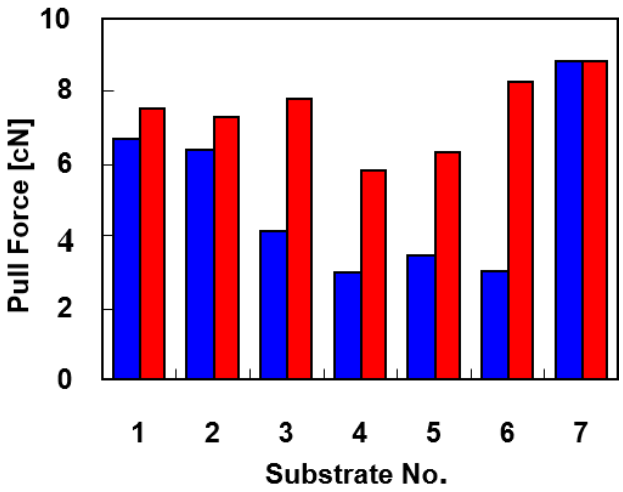

Figure 9: Pull Force of different Substrate Materials prior (blue) and after (red) plasma cleaning in hydrogen plasma.

A clean surface is a must for any type of connecting processes. In case of wire bonding, contamination may, for example, arise from outgassing during die bond curing. For substrate cleaning we use a hot cathonde low voltage plasma source with hydrogen or nitrogen gas for the plasma chemical cleaning. Due to the low Ion energies, no plasma physical cleaning, that is, sputtering occurs.

As cleaned dice ans substrates exhibit excellent wire bondability with large and reproducible pull and shear strength value.

Bond Quality Analysis:

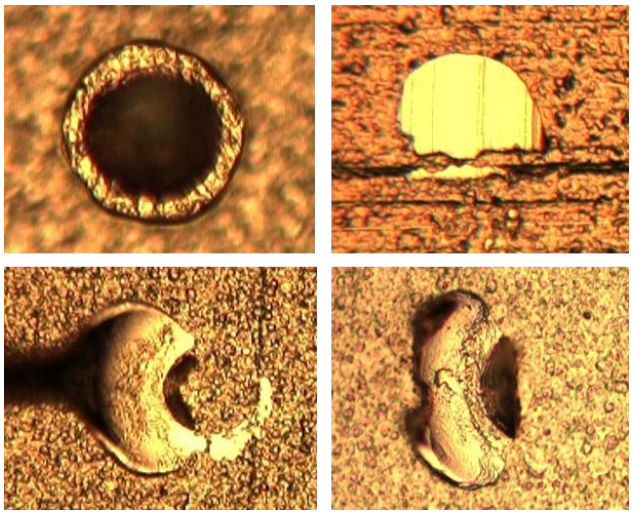

Figure 10: Fig: 10: Ball and Wedgbond pror and after pulling and shearing, respectively.

Our company also offers wire pull and ball shear test data to enable qualification of the wire bond process.

PCB layout and review service

A wire bonding process starts with the correct design and coating of the substrate. Missing fiducials, too small bonding pads or a not suited coating may drastically increase production costs or make it impossible at all.

We offer both, a complete layouting and procurement service, or a review and design support service, depending on your needs.

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COB Infrastructure:

- ESEC 3088
- ESEC 3088IP
- ESEC 3200
- KnS Manual
- UCP Plasma Cleaner
- Dage Pull and Shear Tester
- Nikon optical Microscope with um x,y,z measurement system
- Bonding Tools: > 200 different capillaries

Wire Bond Technologies:

- Wire diameters: 15 to 50µm
- Wire materials: gold
- Fine pitch capability: 40µm
- Minimum loop height: 100µm (standard and worked loops)
- Bond area: 56mm x 80mm
- Accuracy: +/- 2.0µm
- Looping capability: standard and worked (Staggered, CSP, J Wire)
- Ball/Stud bumping

Applications:

- LED
- CMOS camera
- Sensor
- ASIC
- Multi chip module
- MEMS

Customer benefits:

- Substrate Layouting
- COB Assembly (die bonding, wire bonding, plasma cleaning, encapsulation, final testing)
- Prototyping and mass production service
- Wirebondability analysis of PCB and new coating technologies
- Setup of wire bond programs for third partner

Contact

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